In the Claims: This listing of the claims replaces all previous listings.

Please amend the claims as follows:

1-23. (canceled)

24. (currently amended) A memory unit comprising:
- at least two memory areas for storing data,
- first terminals for accessing data within the memory areas,
- second terminals for accessing data within the memory areas, and
- at least two access controllers ~~for~~ selectively providing:
- sole addressing and accessing data through one of the terminals, ~~or~~and
- individual addressing and accessing data through each of the terminals, respectively,
- wherein in case of sole addressing and accessing the data, the access controllers provide access to all of the at least two memory areas by control ports and address ports of only one of the terminals and provide the data within all of the at least two memory areas through data ports of both terminals.

25. (previously presented) The memory unit of claim 24, wherein three memory areas are provided, and wherein a third memory area provides access by the control ports and the address ports of both of the terminals, respectively, and the data through the data ports of both of the terminals, respectively.

26. (previously presented) The memory unit of claim 25, wherein two of the three memory areas provide access by the control ports and the address ports of the terminals, respectively, and the data through the data ports of the terminals, respectively.

27. (previously presented) The memory unit of claim 25, wherein the access controllers provide prioritised access to the third memory area through one of the terminals.

28. (previously presented) The memory unit of claim 24, wherein the first and/or second terminal comprises control ports for receiving control signals for controlling access to the memory areas.

29. (previously presented) The memory unit of claim 24, wherein the first and/or second terminal comprises address ports for receiving addressing signals for addressing data within the memory areas.

30. (previously presented) The memory unit of claim 29, wherein the address ports provide access to an external address bus.

31. (previously presented) The memory unit of claim 24, wherein the first and/or second terminal comprises data ports for reading and/or writing data to and/or from the memory areas.

32 (previously presented) The memory unit of claim 24, wherein the access controllers provide access to the data areas based on control and/or address signals at said terminals.

33. (previously presented) The memory unit of claim 24, wherein the access controllers are state machines, the state machines providing access to the data areas based on states of signals at the first and second terminals.

34. (previously presented) The memory unit of claim 24, wherein the access controllers comprise memory registers.

35. (previously presented) The memory unit of claim 24, wherein the access controllers provide access to at least one memory area by the control ports and the address ports of the terminals, respectively, and provide the data through the data ports of the terminals, respectively, in case of individual addressing.

36. (previously presented) The memory unit of claim 35, wherein the access controllers provide access to at least one memory area by both of the control ports and the address ports of the terminals, and provide the data through the data ports of the terminals, respectively, in case of individual addressing.

37. (previously presented) The memory unit of claim 24, wherein at least two memory areas are provided.

38. (previously presented) The memory unit of claim 24, wherein programming the size of the memory areas is provided through one of the terminals.

39. (previously presented) The memory unit of claim 24, wherein one of the terminals provides accessing the data by a central processing unit, and wherein one of the terminals provides accessing the data by a graphics processor.

40. (previously presented) The memory unit of claim 24, wherein the bandwidth and/or clocking frequency for the terminals is different.

41. (currently amended) A method comprising:

- receiving access signals and providing data from memory areas for storing data through first terminals,
- receiving access signals and providing data from said memory areas through second terminals, and
- selectively receiving access signals solely through one of said first and second terminals and providing data from memory areas through both said first and second terminals, ~~or~~ and
- receiving access signals and providing data from memory areas through both of said first and second terminals individually, respectively,
- wherein in case of sole addressing and accessing the data, the providing access to all of the at least two memory areas is by control ports and address ports of only one

of the first and second terminals and the data within all of the at least two memory areas is provided through data ports of both of said first and second terminals.

42. (currently amended) A system for providing memory comprising:
- a first processor in communication with a memory unit, and a second processor in communication with the memory unit,
- at least two access controllers ~~for~~ selectively providing:
- sole addressing and accessing data by one of the processors, ~~or~~and
- individually addressing and accessing data by each of the processors, respectively,
- wherein in case of sole addressing and accessing the data, the access controllers provide access to all of the at least two memory areas by control ports and address ports of only one of said first and second processors and provide the data within all of the at least two memory areas through data ports of both of said first and second processors.

43. (previously presented) A module for providing memory to processors, comprising connection terminals providing communication between an electronic circuit and a memory unit according to claim 24.

44. (previously presented) A mobile communication device comprising a memory unit according to claim 24.

45. (currently amended) A memory unit comprising:
- at least first and second means for storing data,
- first means for accessing data within the first and second means for storing data, and
- second means for accessing data within the first and second means for storing data, and
- means for selectively providing
- sole addressing and accessing data through one of the first and second means for accessing data, ~~or~~and

- individual addressing and accessing data through each of the first and second means for accessing data, respectively,
- wherein in case of sole addressing and accessing the data, said means for selectively providing access to the first and second means for storing data is by control ports and address ports of only one of the first and second means for accessing data within all of the at least two memory areas and provides the data within all of the at least two memory areas through data ports of both the first and second means for accessing data.

46. (previously presented) The memory unit of claim 45, wherein three means for storing data are provided, and wherein the third means for storing data provides access by the control ports and the address ports of both of the first and second means for accessing data, respectively, and the data through the data ports of both of the first and second means for accessing data, respectively.

47. (new) The method of claim 41, wherein three memory areas are provided, and wherein a third memory area is accessed by the control ports and the address ports of both of the terminals, respectively, and the data through the data ports of both of the terminals, respectively.

48. (new) The method of claim 47, wherein two of the three memory areas are accessed by the control ports and the address ports of the terminals, respectively, and the data through the data ports of the terminals, respectively.

49. (new) The method of claim 47, wherein the access controllers prioritizedly accesses the third memory area through one of the terminals.

50. (new) The method of claim 41, wherein control signals for controlling access to the memory areas are received by control ports of the first and/or second terminal.

51. (new) The method of claim 41, wherein addressing signals for addressing data within the memory areas are received by address ports of the first and/or second terminal.

52. (new) The method of claim 51, wherein an external address bus is accessed by the address ports provided.

53. (new) The method of claim 41, wherein data to and/or from the memory areas is read and/or written by data ports of the first and/or second terminal.

54. (new) The method of claim 41, wherein the access controllers access the data areas based on control and/or address signals at said first and second terminals.

55. (new) The method of claim 41, wherein the access controllers are state machines, the state machines accessing the data areas based on states of signals at the first and second terminals.

56. (new) The method of claim 41, wherein the access controllers accesses at least one memory area by the control ports and the address ports of the terminals, respectively, and provide the data through the data ports of the terminals, respectively, in case of individual addressing.

57. (new) The method of claim 56, wherein the access controllers access at least one memory area by both of the control ports and the address ports of the terminals, and provide the data through the data ports of the terminals, respectively, in case of individual addressing.

58. (new) An apparatus, comprising:
- at least two memory areas for storing data,
- first terminals for accessing data within the memory areas,
- second terminals for accessing data within the memory areas, and
- at least two access controllers selectively providing:

- sole addressing and accessing data through one of the terminals, and
- individual addressing and accessing data through each of the terminals, respectively,
- wherein in case of sole addressing and accessing the data, the access controllers provide access to both of the at least two memory areas by control ports and address ports of only one of the terminals and provide the data within both of the at least two memory areas through data ports of both terminals.